

FIG. 1

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Burst Length	Starting Column Address			Linear	Interleave
	A ₂	A ₁	A ₀		
2	V	V	0	0-1	0-1
	V	V	1	1-0	1-0
4	V	0	0	0-1-2-3	0-1-2-3
	V	0	1	1-2-3-0	1-0-3-2
	V	1	0	2-3-0-1	2-3-0-1
	V	1	1	3-0-1-2	3-2-1-0
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
8	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

FIG. 2

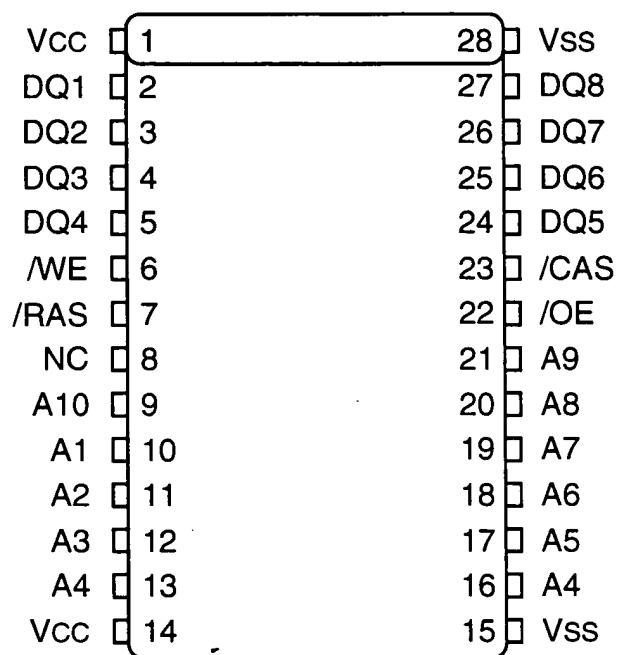


FIG. 3

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30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F

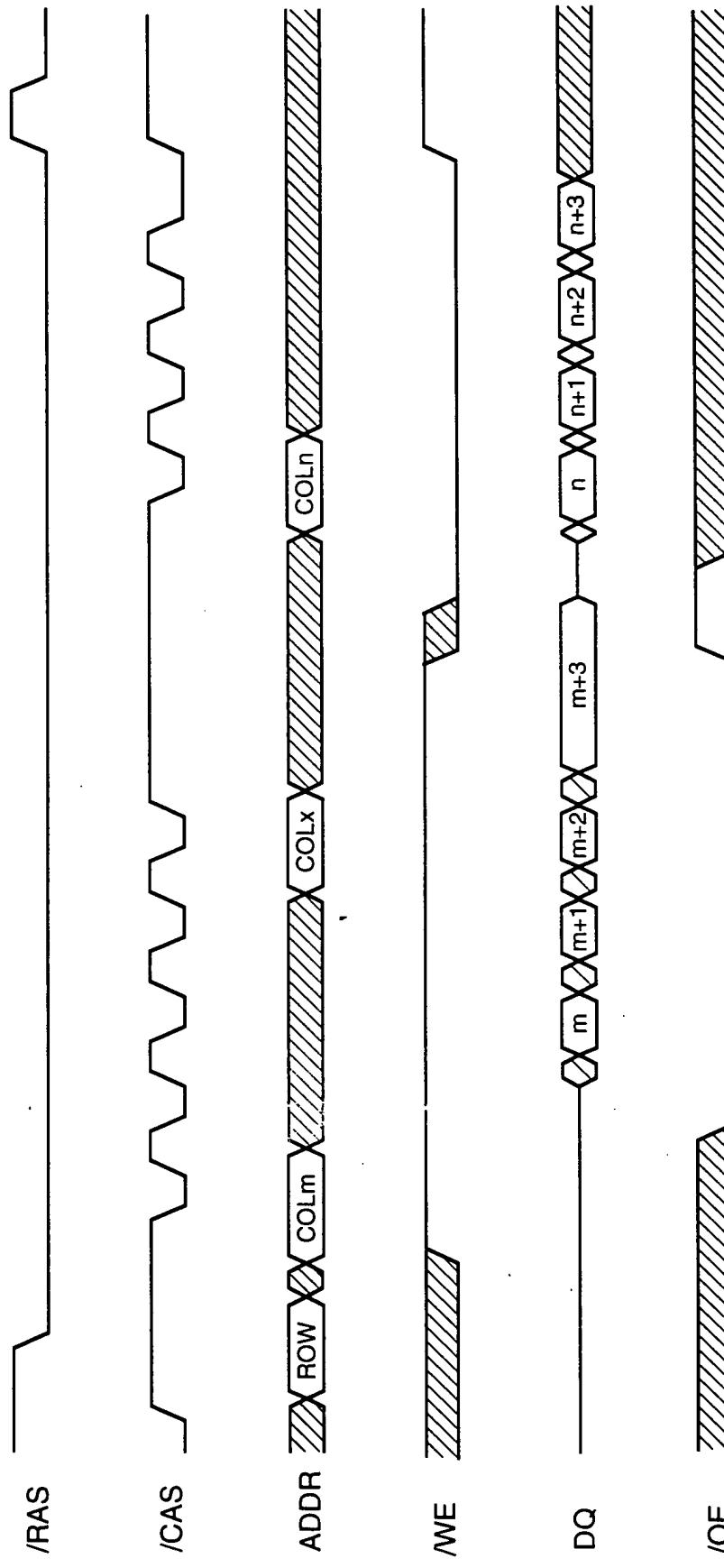


FIG. 4

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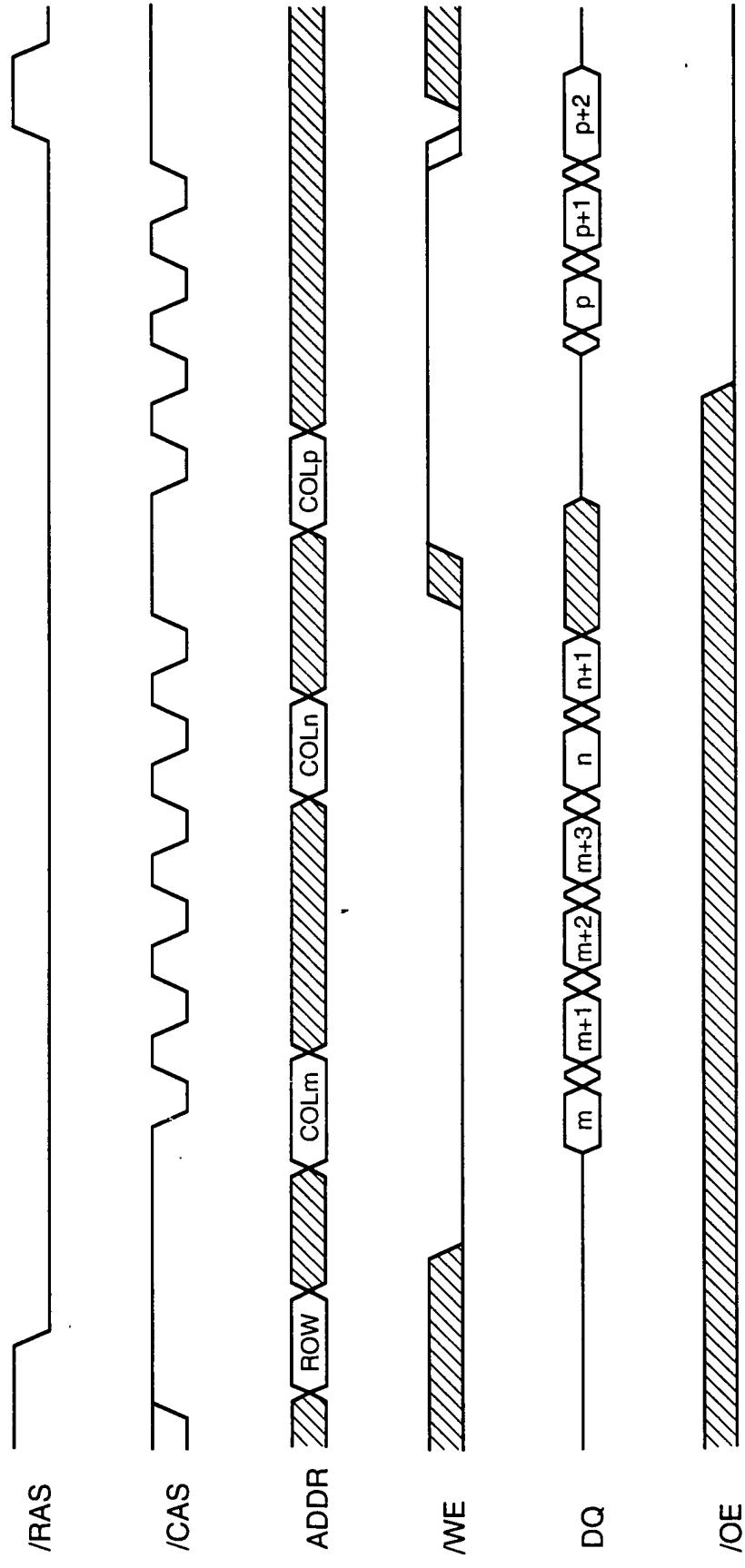


FIG. 5

00000000000000000000000000000000

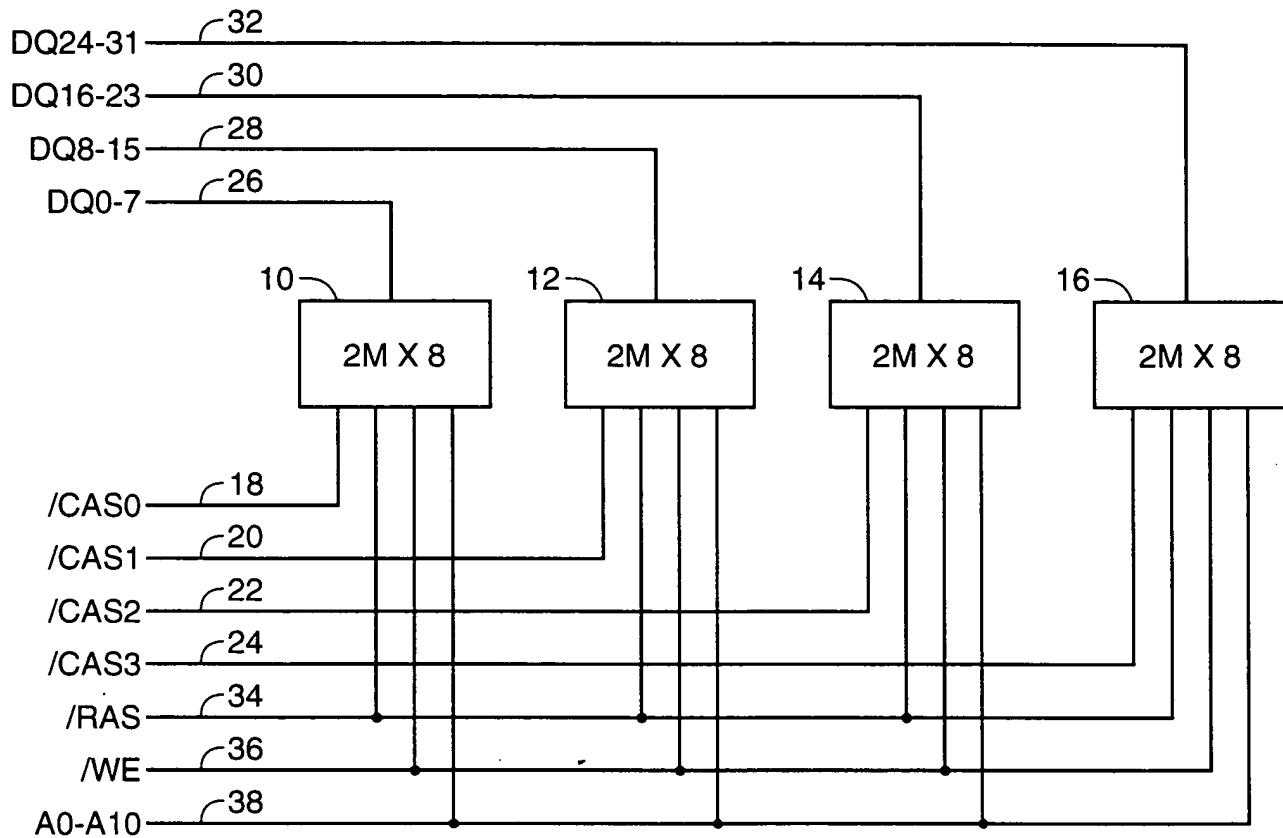


FIG. 6

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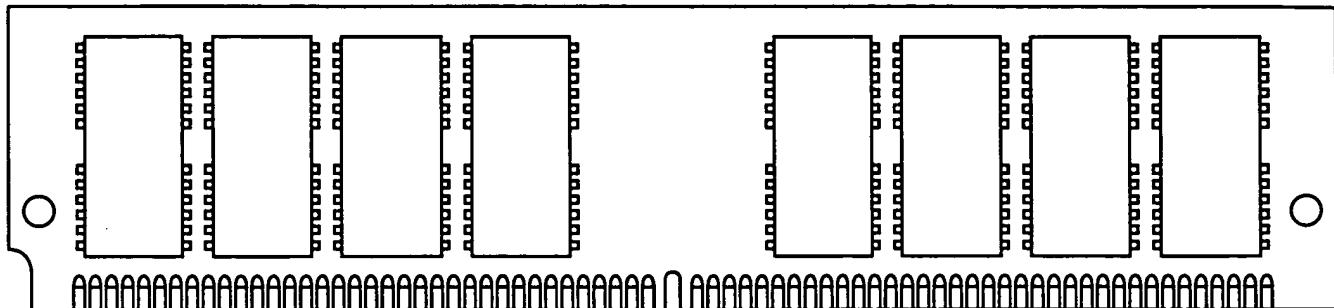


FIG. 7

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PIN #	SYMBOL						
1	Vss	19	A10	37	NC	55	DQ12
2	DQ1	20	DQ5	38	NC	56	DQ28
3	DQ17	21	DQ21	39	Vss	57	DQ13
4	DQ2	22	DQ6	40	/CAS0	58	DQ29
5	DQ18	23	DQ22	41	/CAS2	59	VCC
6	DQ3	24	DQ7	42	/CAS3	60	DQ30
7	DQ19	25	DQ23	43	/CAS1	61	DQ14
8	DQ4	26	DQ8	44	/RAS0	62	DQ31
9	DQ20	27	DQ24	45	/RAS1	63	DQ15
10	VCC	28	A7	46	/OE	64	DQ32
11	PD5	29	NC	47	/WE	65	DQ16
12	A0	30	VCC	48	PD ECC	66	PD EDO
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ25	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	NC	52	DQ26	70	PD4
17	A5	35	NC	53	DQ11	71	PD refresh
18	A6	36	NC	54	DQ27	72	VSS

FIG. 8

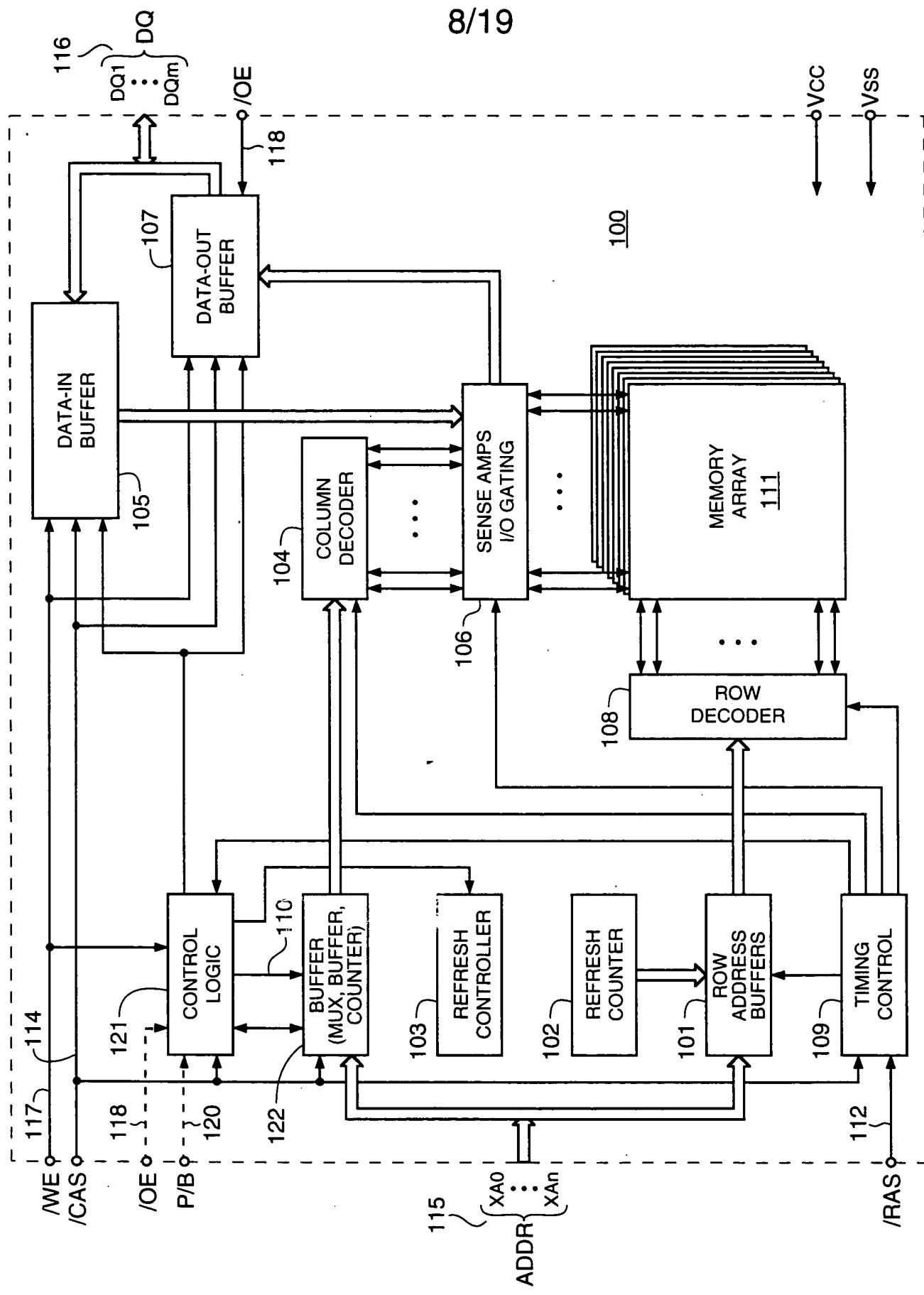


FIG. 9

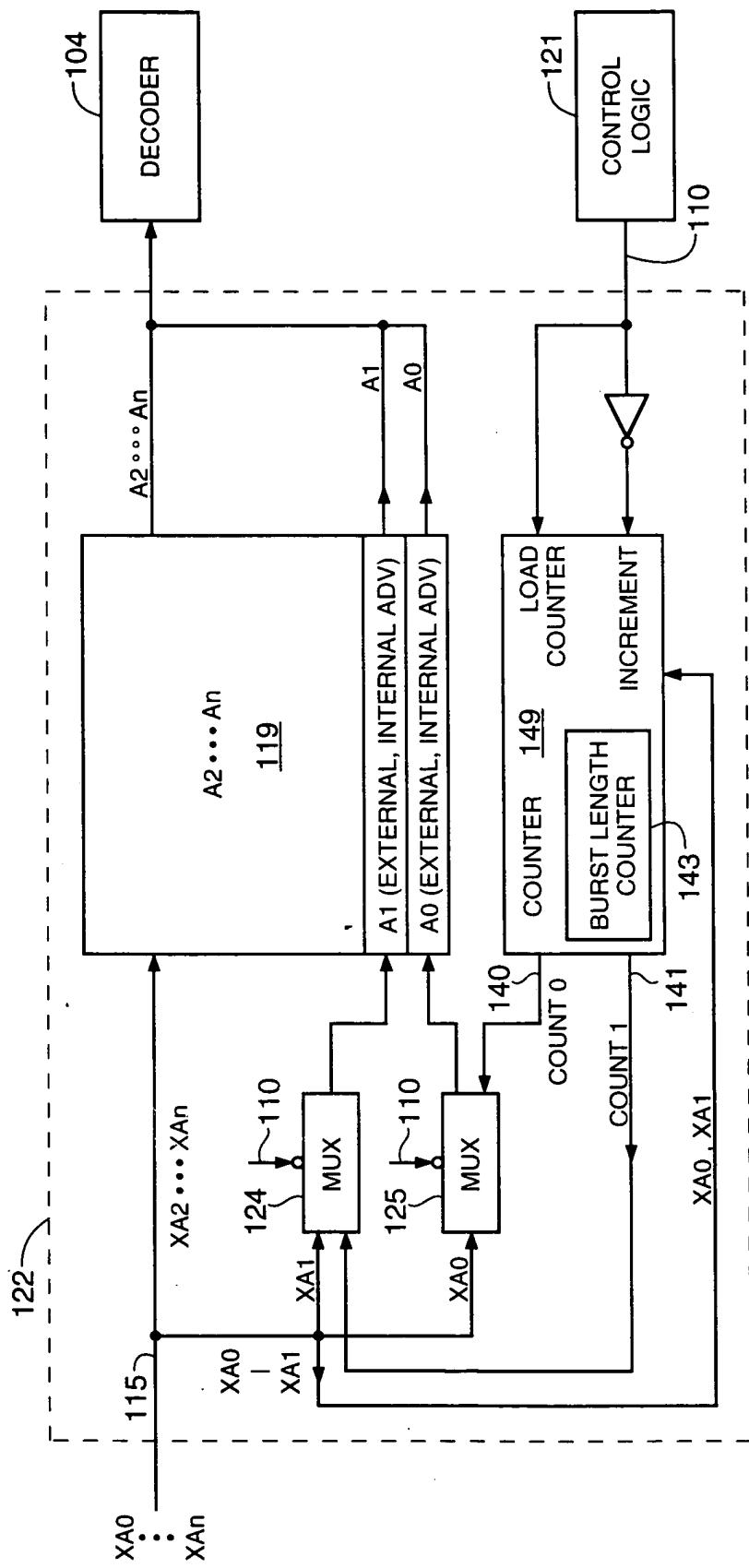


FIG. 10

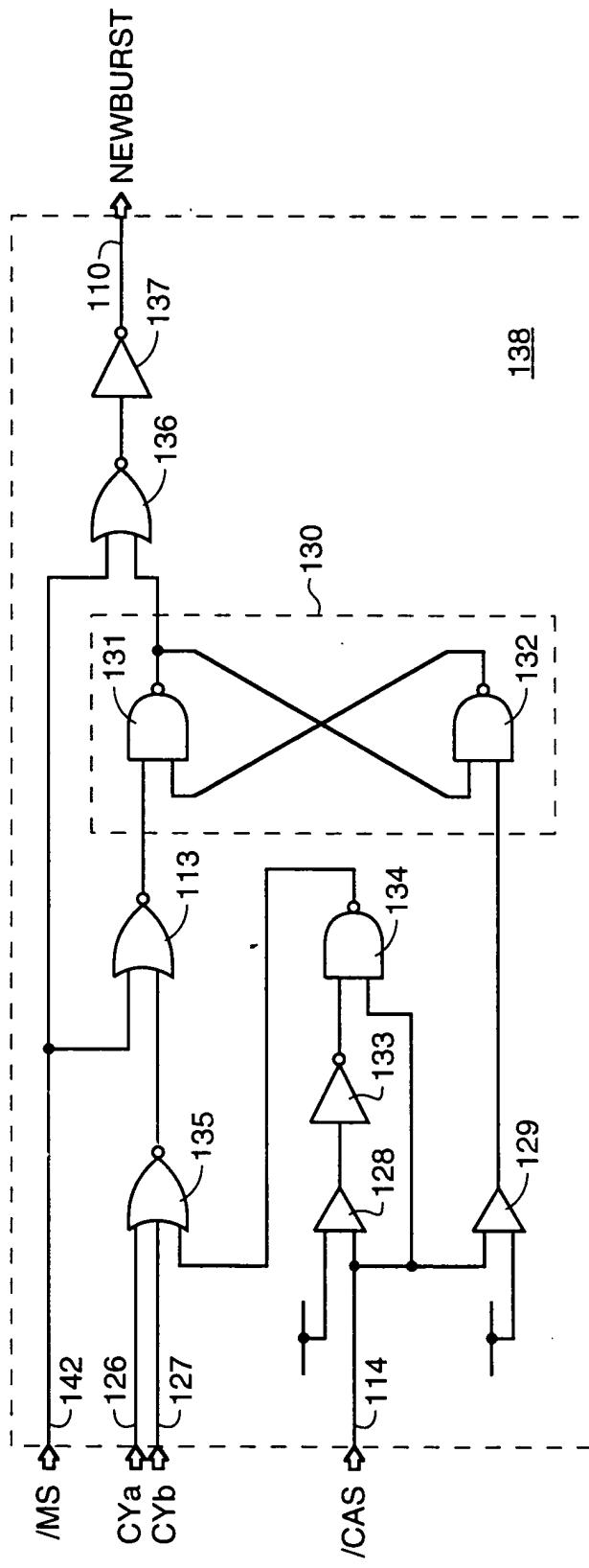


FIG. 11

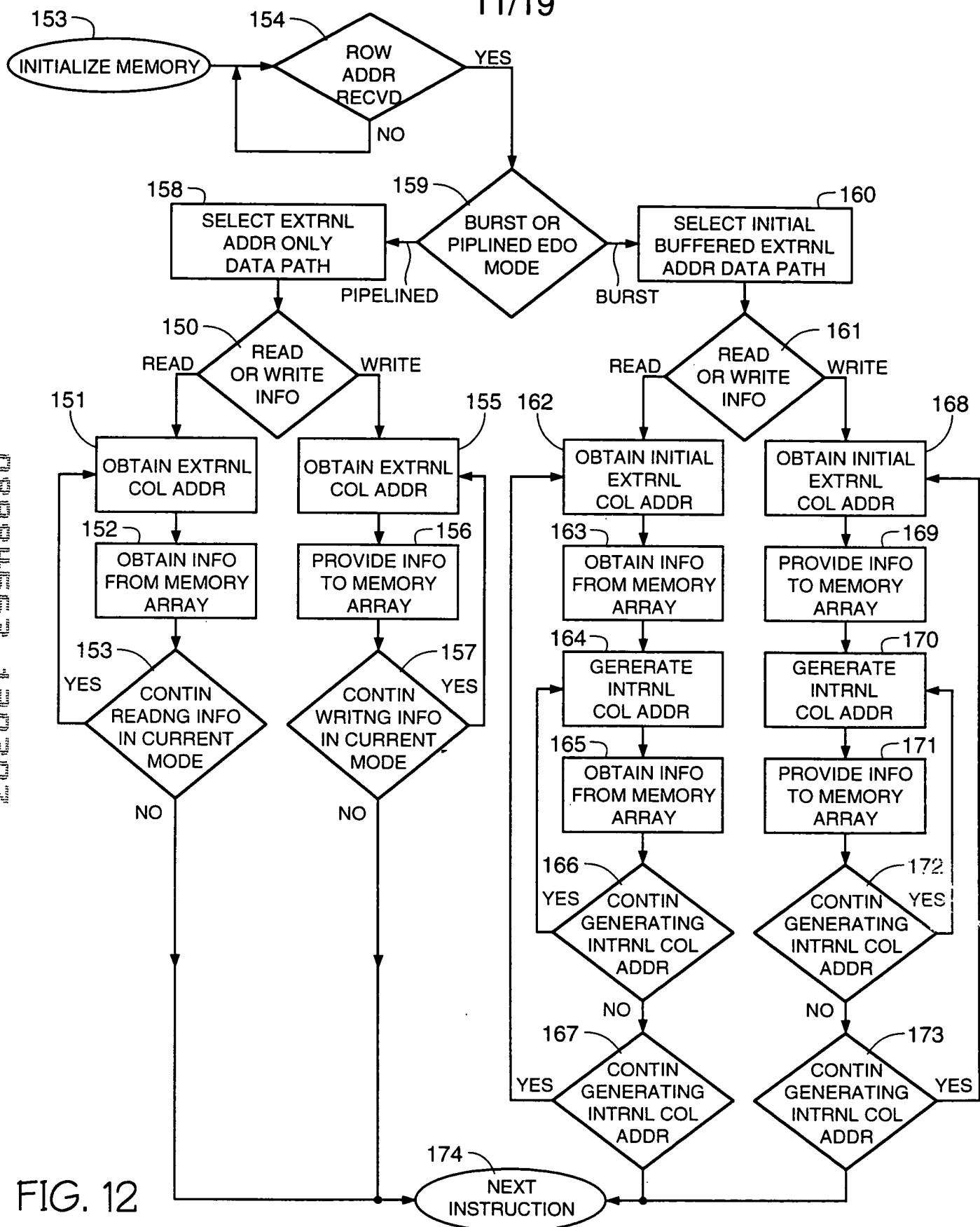


FIG. 12

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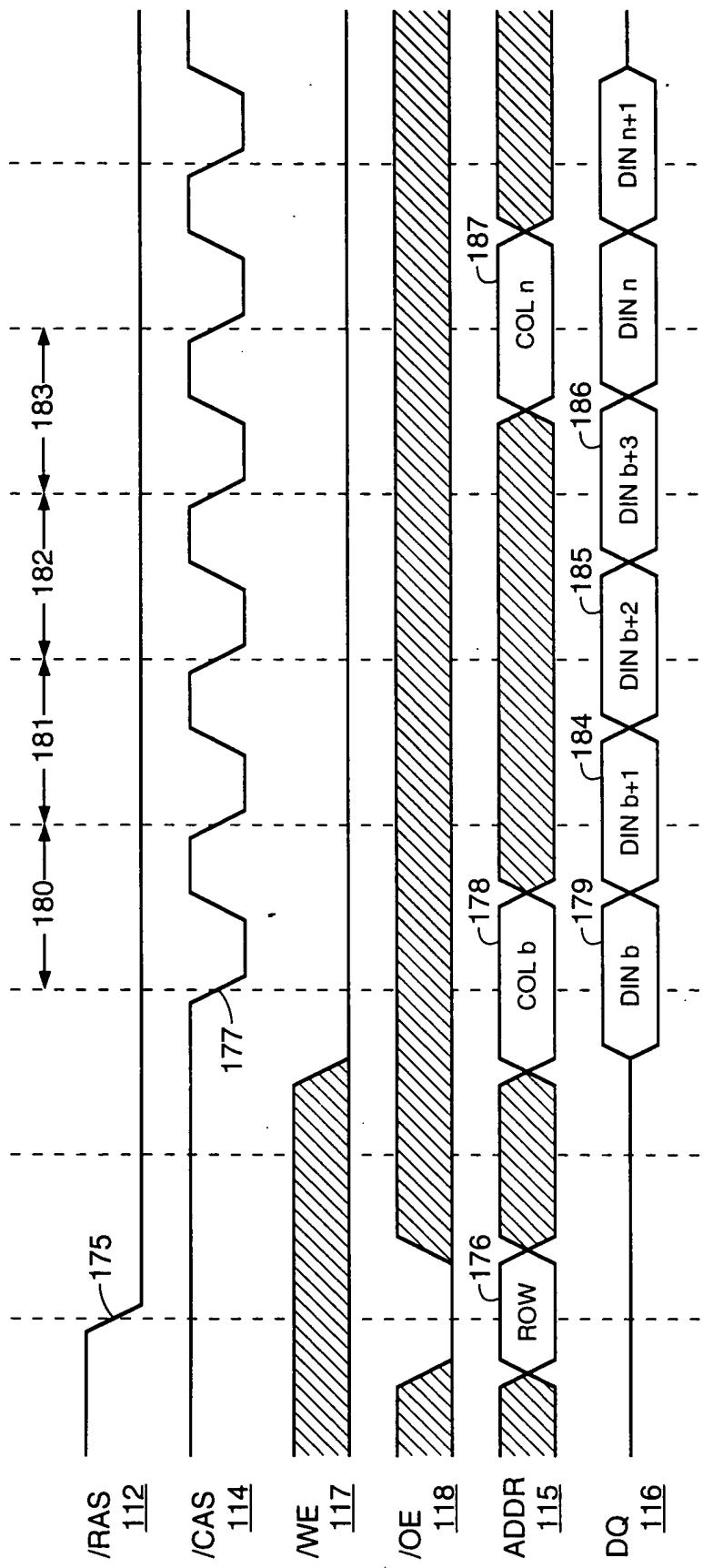


FIG. 13

2' E DEC " Cache 640

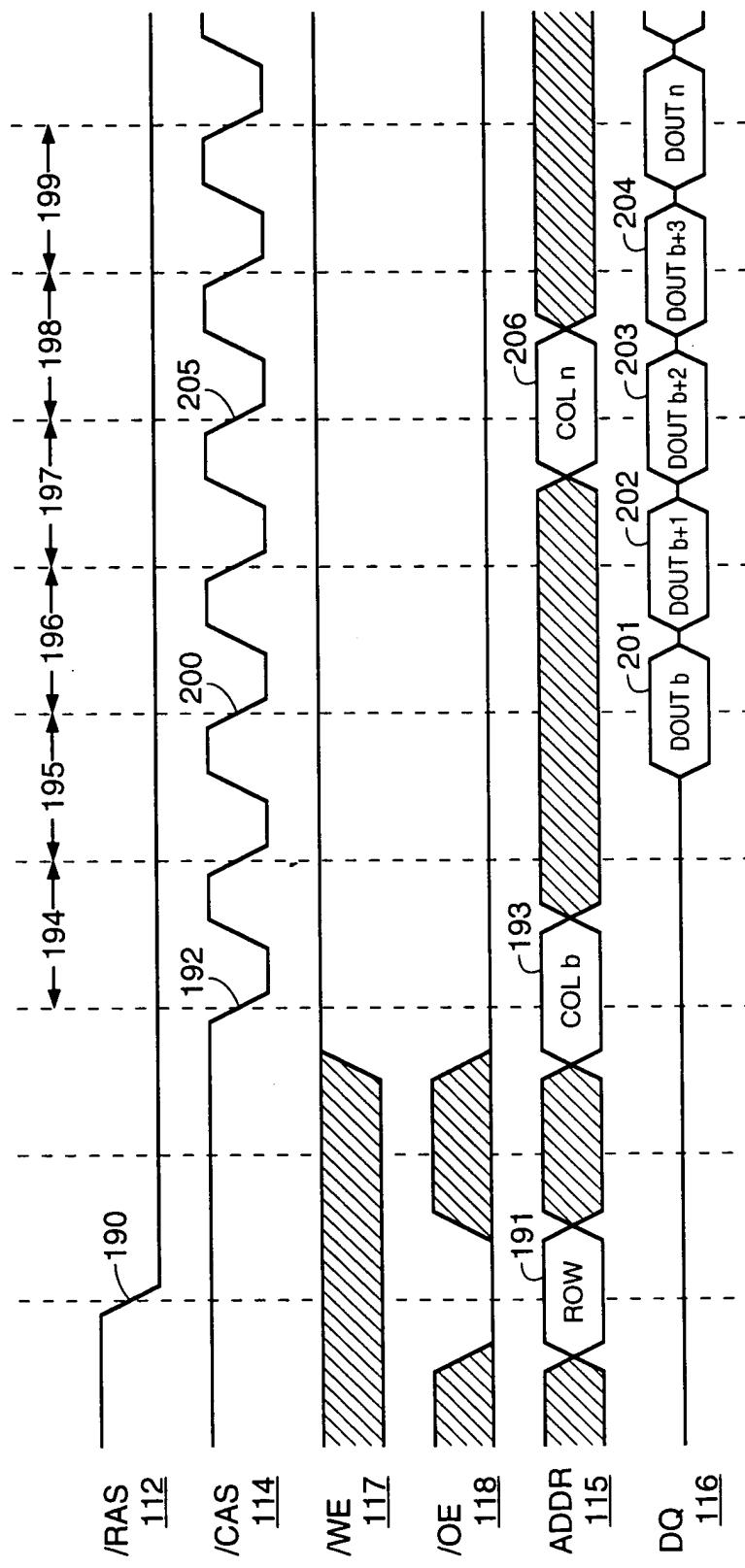


FIG. 14

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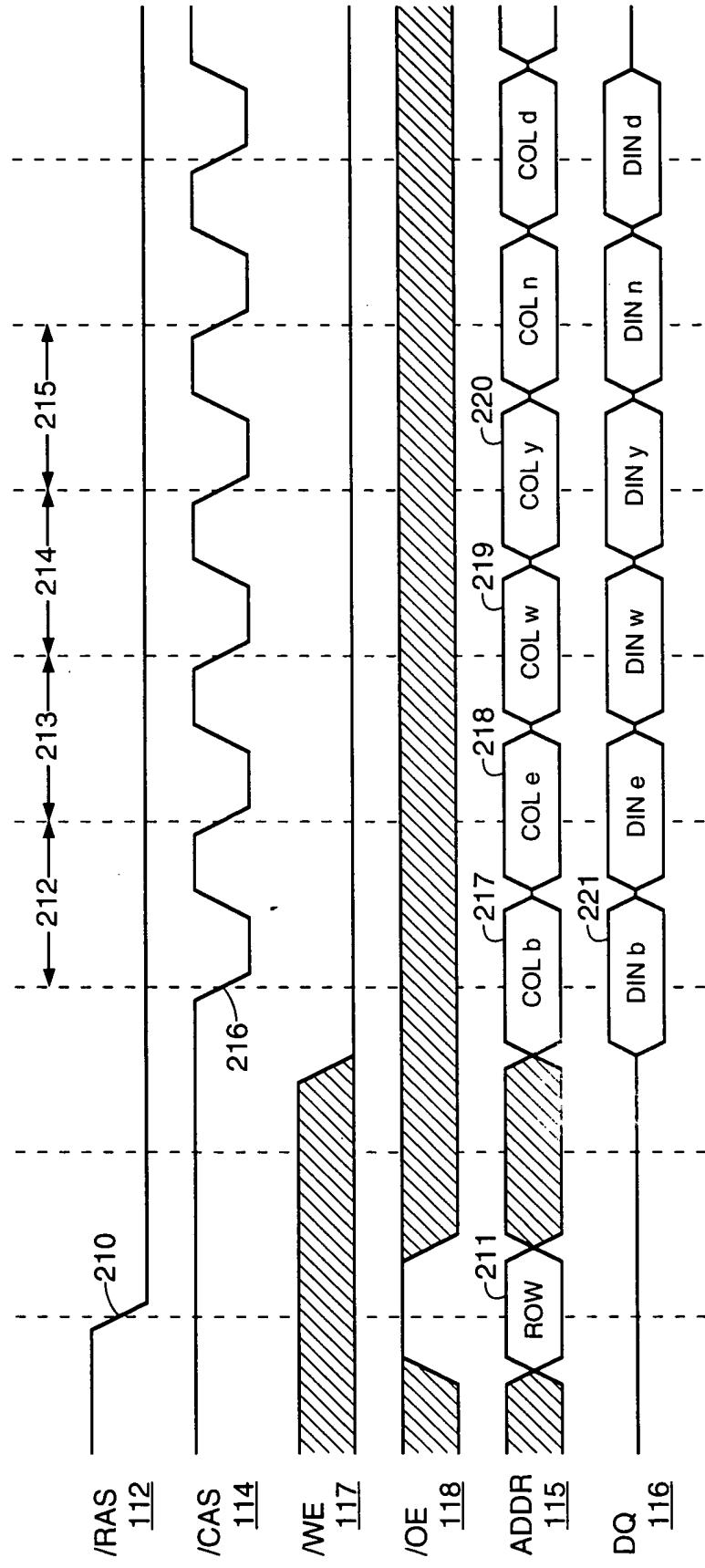


FIG. 15

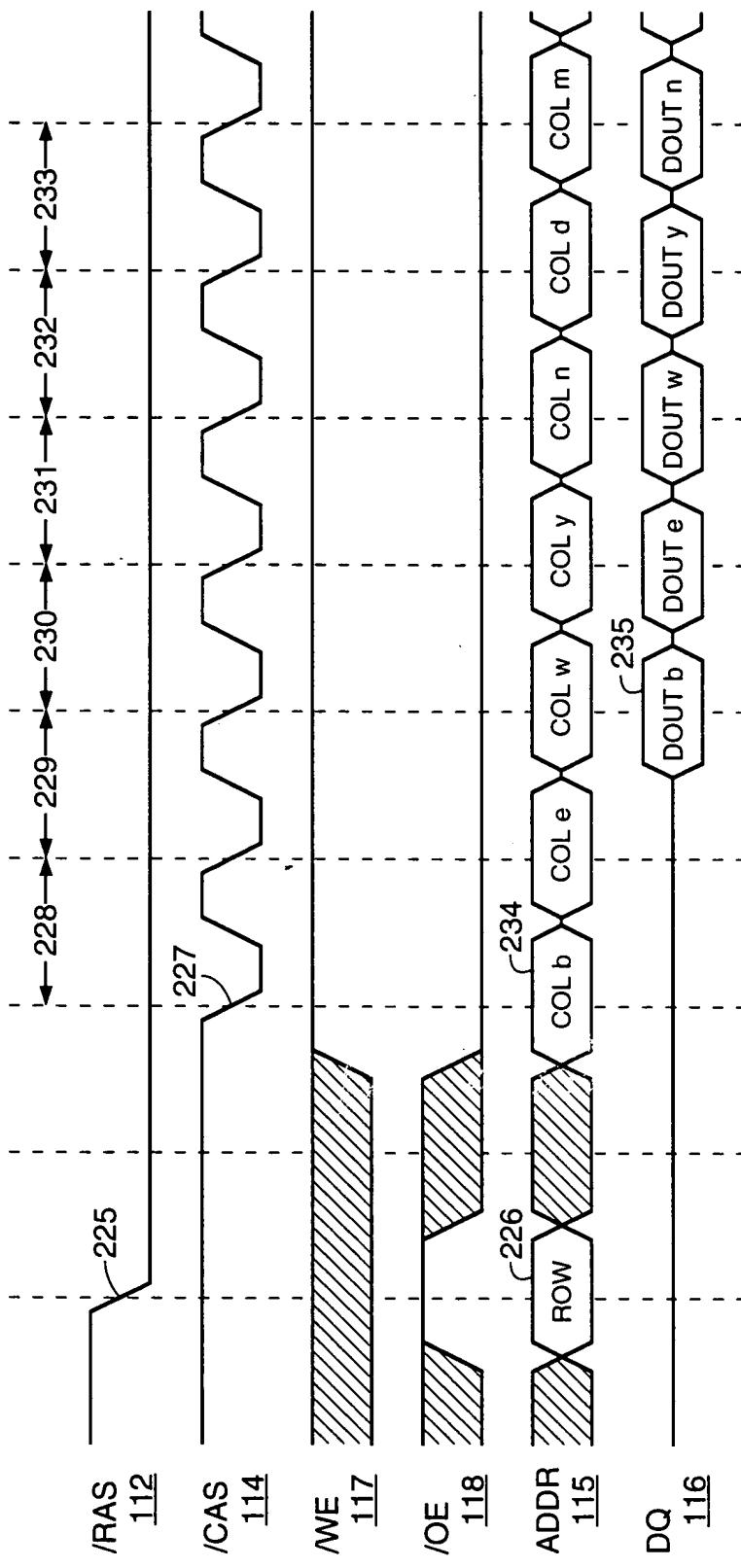


FIG. 16

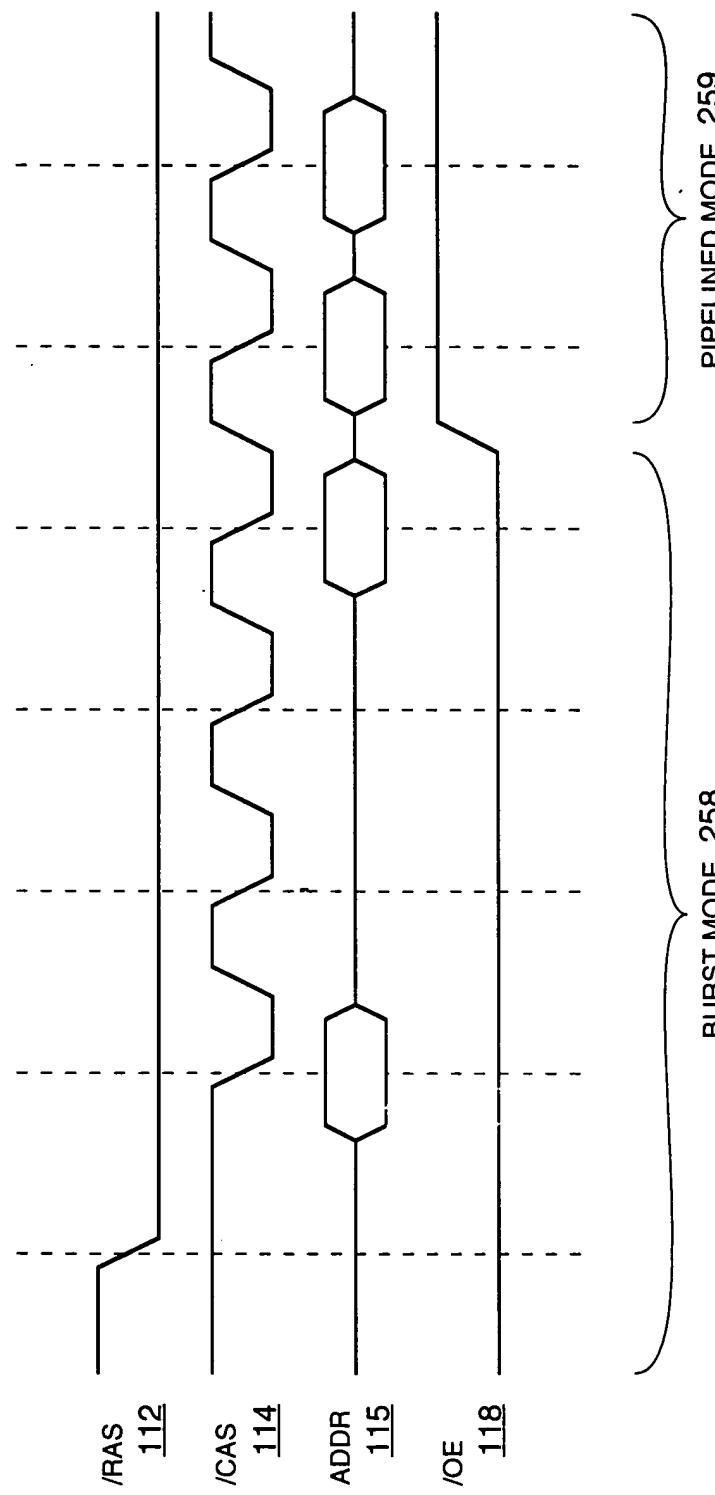


FIG. 17

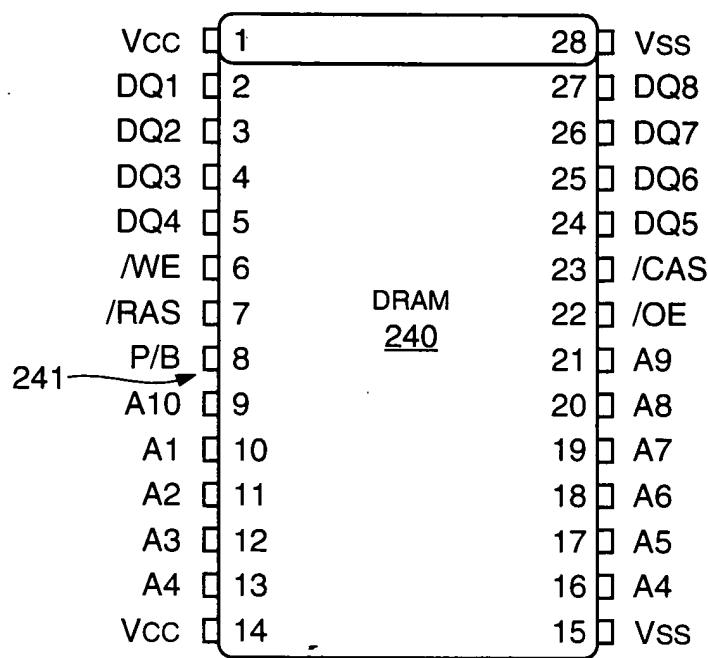


FIG. 18

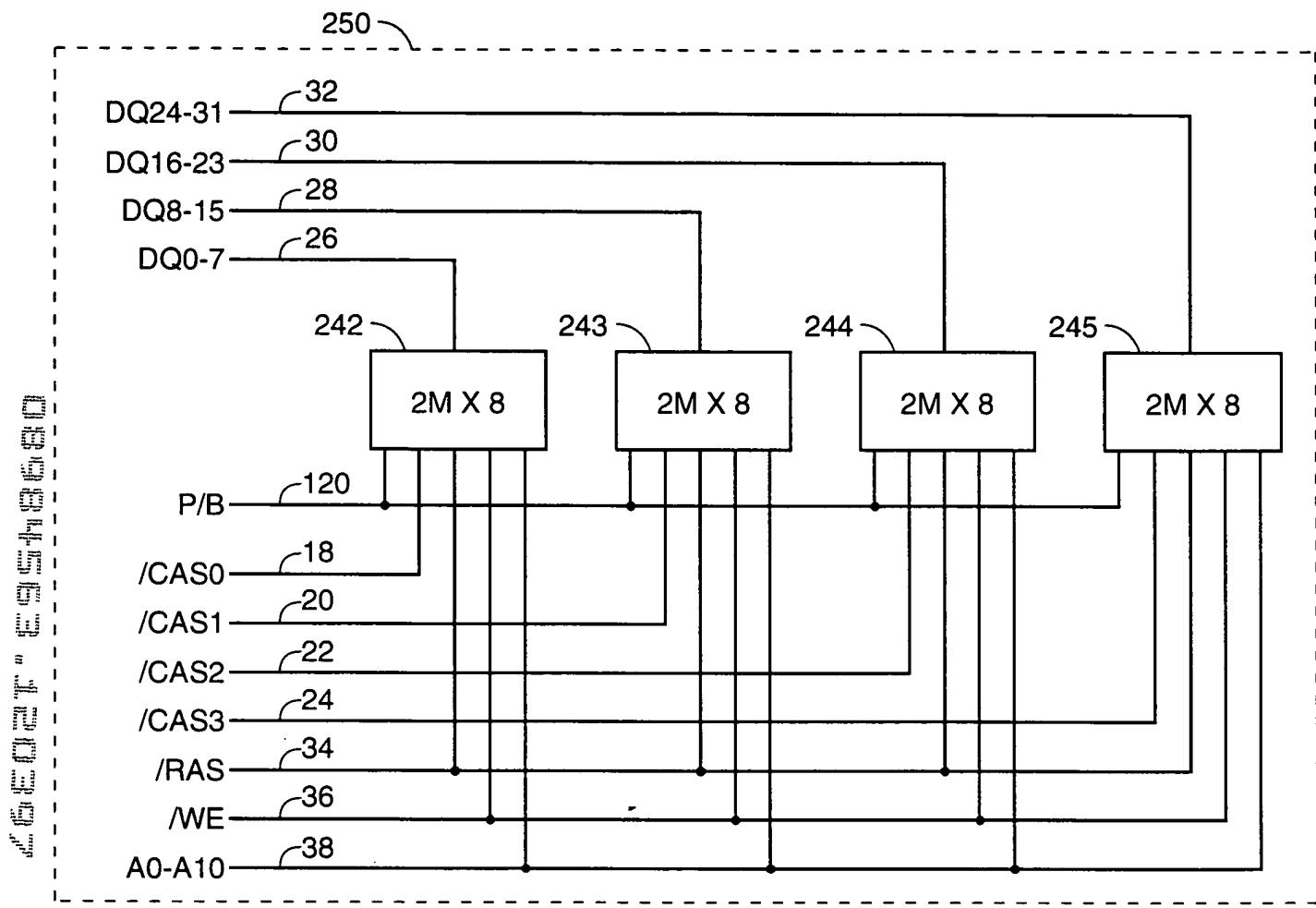


FIG. 19

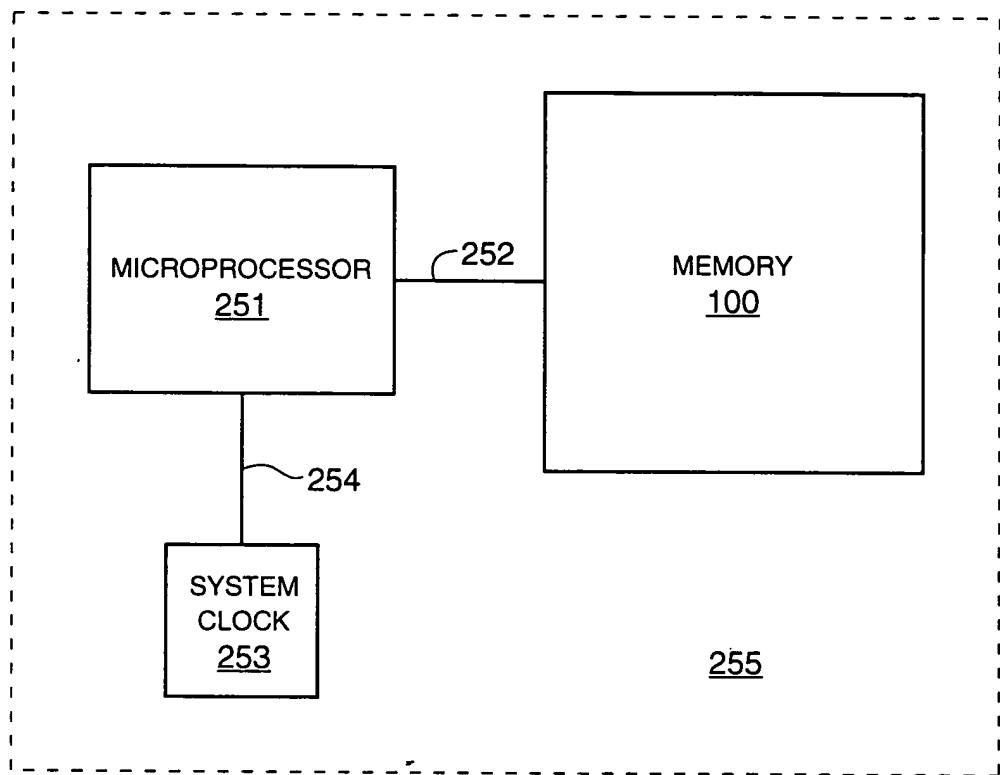


FIG. 20